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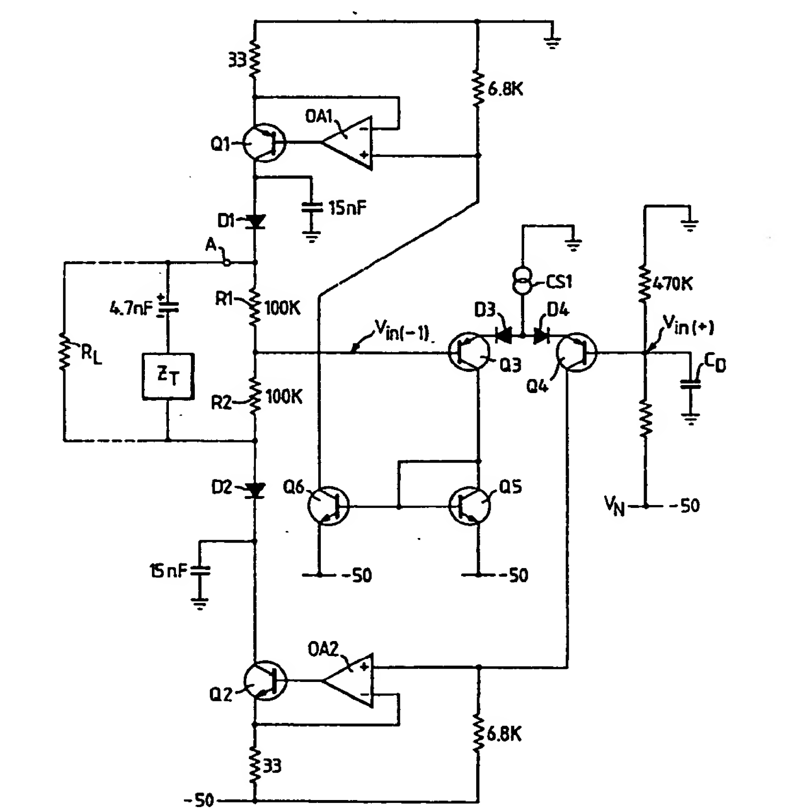
(54) Telephone subscribers' line interface circuit

(57) A line feed amplifier arrangement, for supplying to a telephone line the DC line feed, which is modulated with outgoing speech and AC signals includes as its central element a long-tailed pair (Q3—Q4) with a direct current source (CS1) connected to its commoned emitters via diodes (D3, D4). This current source it is which is modulated with speech and AC signals when in use, but the resulting DC+AC is still unidirectional. One transistor (Q4) of the pair has its base coupled to a reference voltage ($V_{IN(+)}$) while the other (Q3) has its base connected to a voltage ($V_{IN(-)}$) defined by the centre tap of two resistors (R1 and R2) connected across the line (A—B). Thus the long-tailed pair compares these voltages, and the currents which its transistors pass are controlled by the relation between those voltages.

One transistor (Q4) has its collector connected to a current feed device (Q2—OA2) for one wire (B) so to control the current therein. The other transistor (Q3) of the pair has its collector connected to the input of a unity current ratio current mirror (Q6—Q5) the output of which goes to a current feed device (Q1—OA1) for the other wire (A) so as to control the current therein via the current mirror. These current feed devices are amplifiers, so that the control circuit including the long-tailed pair (Q3—Q4) is a low power circuit. Thus the current supply to the line is controlled on the basis of the comparator action referred to, and by the current from the current source.

Fig.3.



The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

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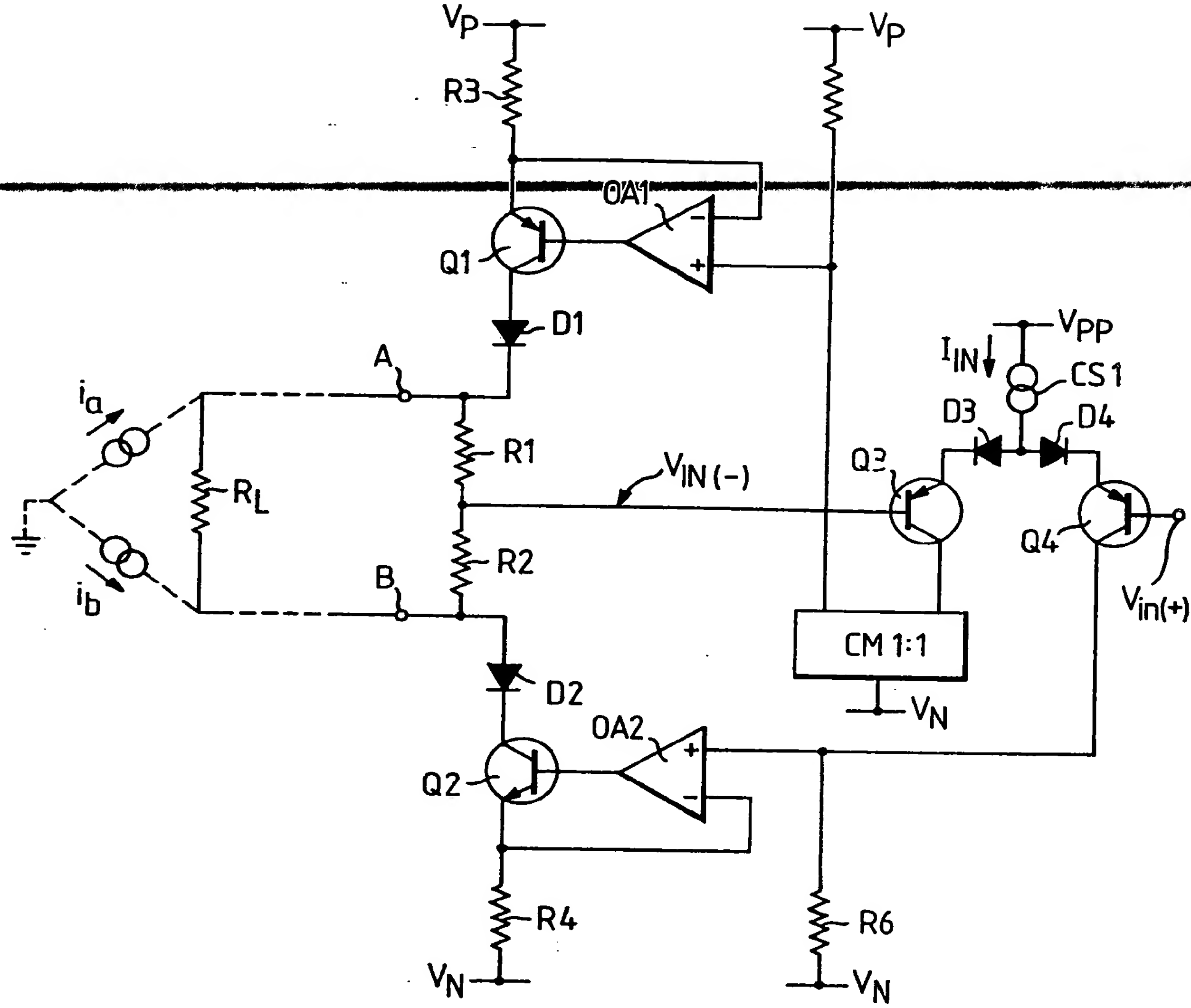
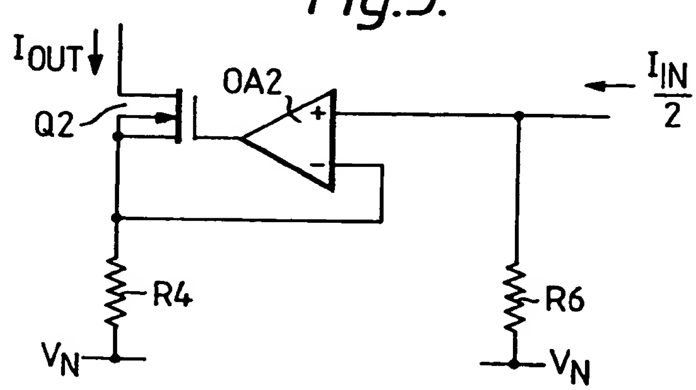
Fig.1.



VP
VP
R3
OA1
Q1
D1
VPP
IIN
CS1
A
D3
D4
ia
Q3
Q4
R1
VIN(-)
RL
R2
B
ib
Vin(+)
CM 1:1
VN
D2
OA2
Q2
R4
R6
VN
VN

Fig.5.



IOUT
OA2
IIN
2
Q2
R4
R6
VN
VN

Fig.2.

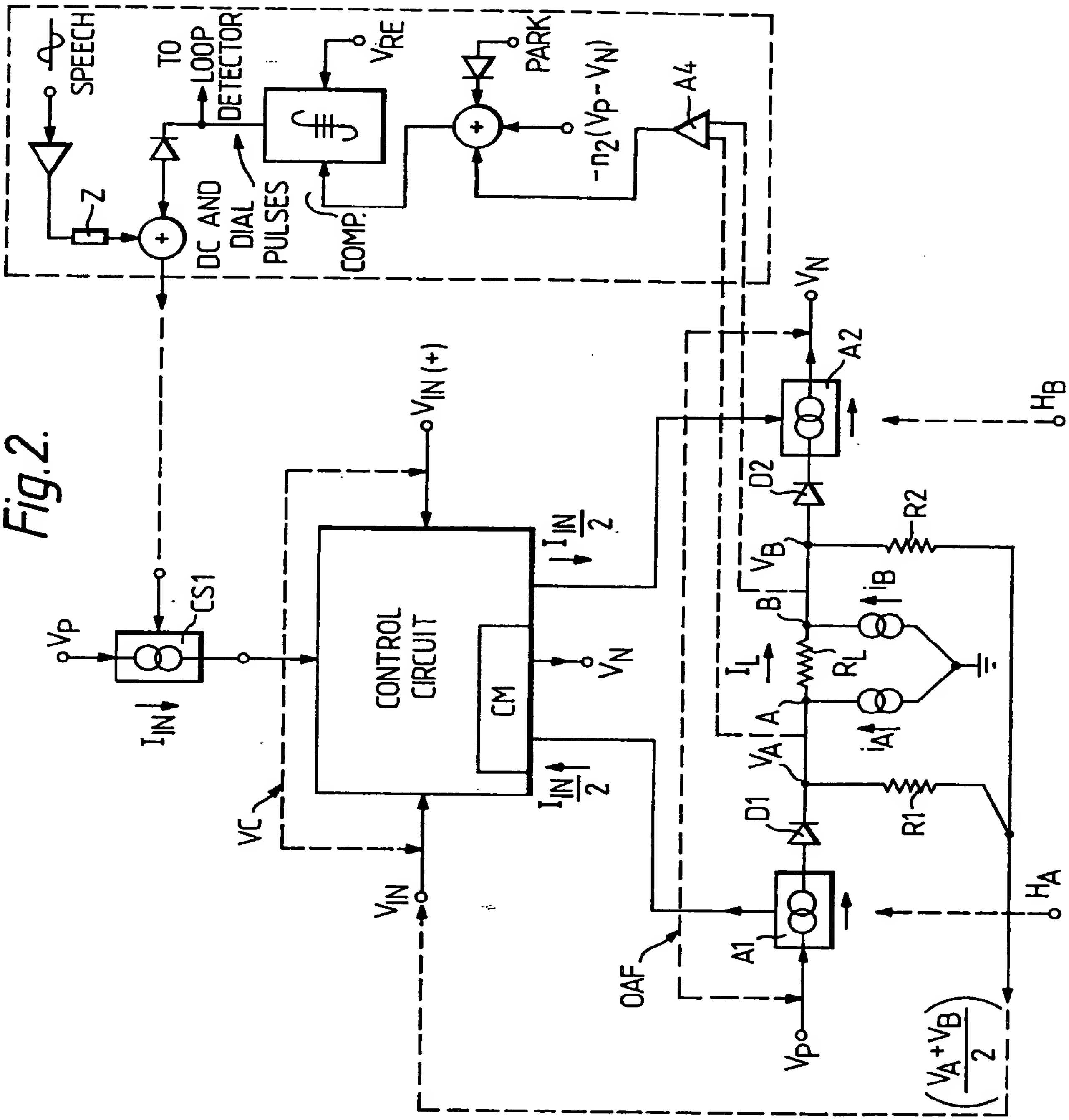

SPEECH
Z
TO LOOP DETECTOR
DC AND DIAL PULSES
COMP.
V_{RE}
PARK
$-n_2(V_P-V_N)$
A4
V_N
A2
H_B
R2
D2
V_B
B
i_B
I_L
R_L
A
V_A
i_A
D1
R1
H_A
A1
OAF
V_P
$\left(\frac{V_A+V_B}{2}\right)$
V_{IN}
VC
CONTROL CIRCUIT
CM
$I_{\frac{IN}{2}}$
$V_{IN}(+)$
CS1
V_P
I_{IN}

Fig.3.

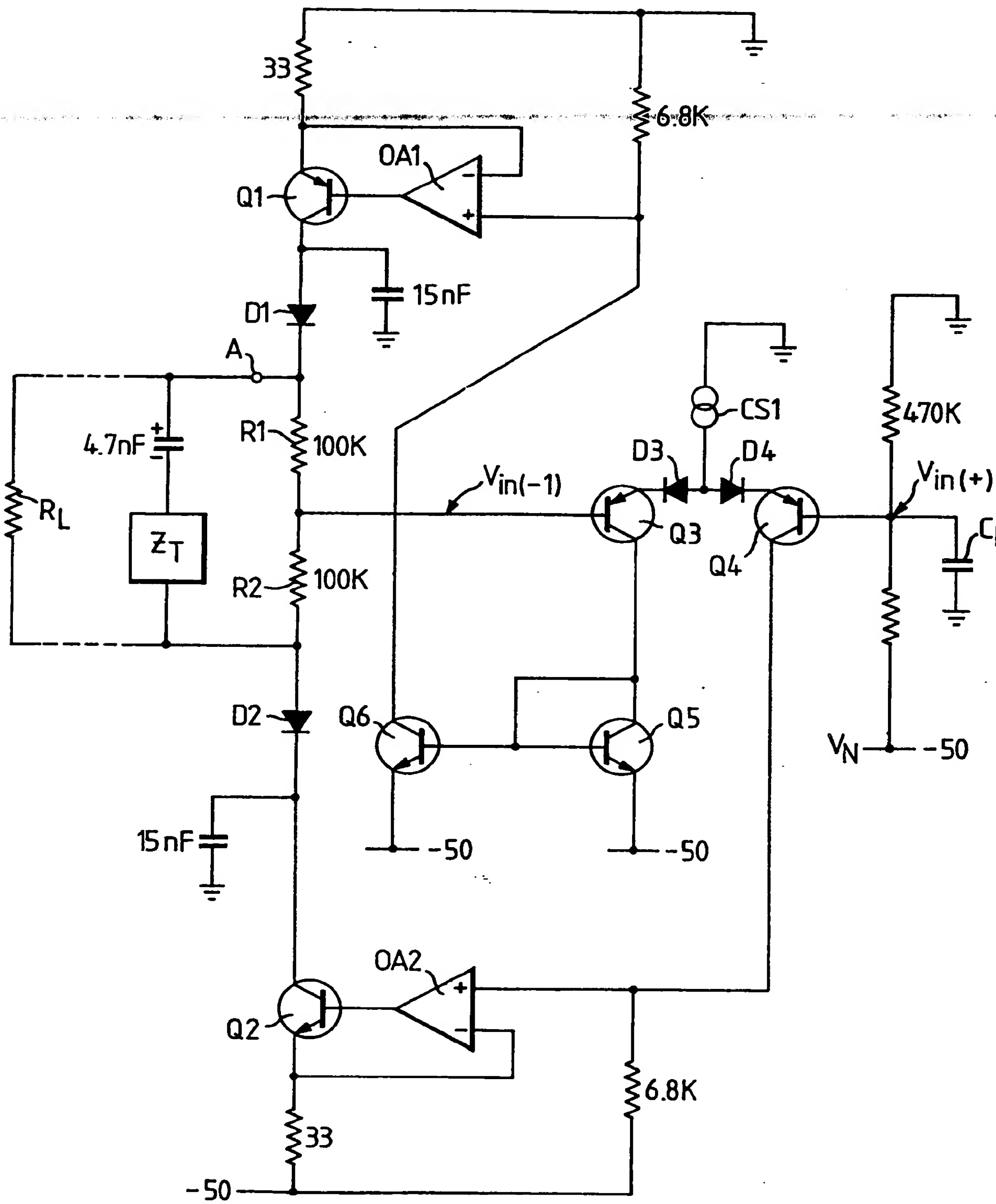

33
6.8K
OA1
Q1
15nF
D1
A
4.7nF
R1
100K
RL
ZT
Vin(-1)
D3
CS1
D4
470K
Vin(+)
Q3
Q4
CD
R2
100K
D2
Q6
Q5
VN
-50
15nF
-50
-50
OA2
Q2
6.8K
33
-50

Fig.4.

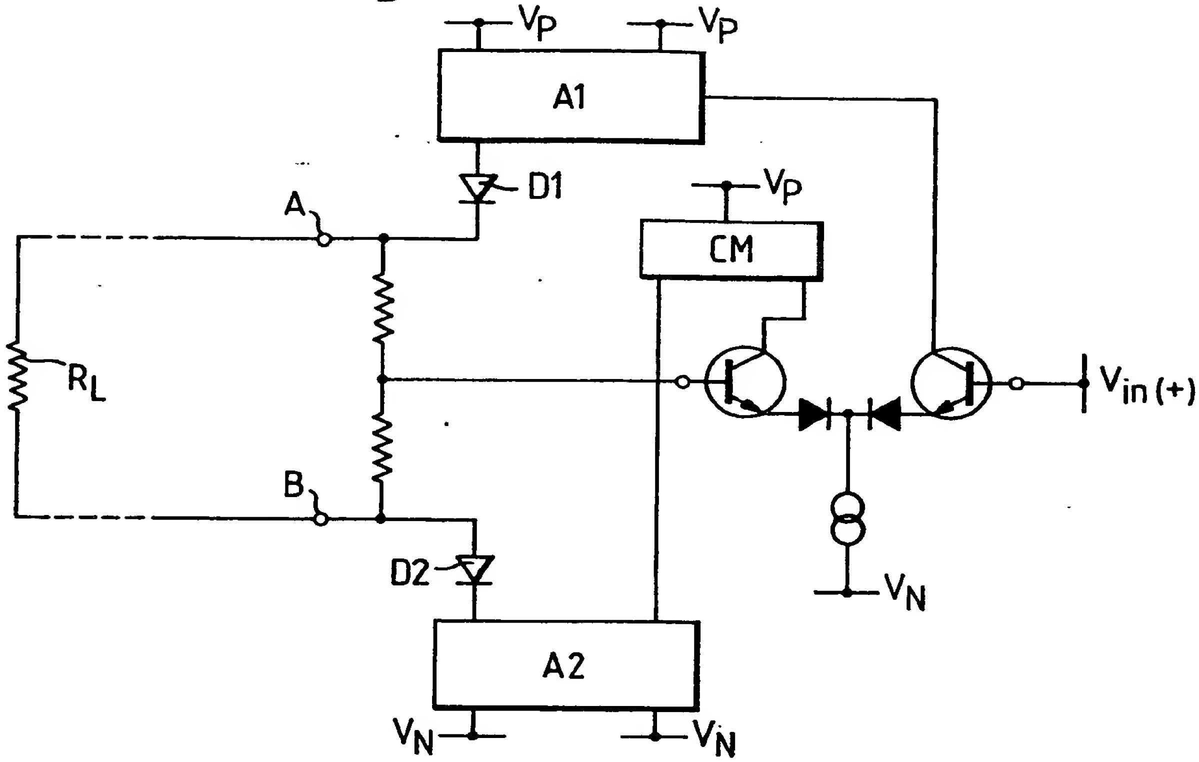

VP
VP
A1
D1
VP
A
CM
RL
Vin (+)
B
D2
VN
A2
VN
VN

Fig.6.

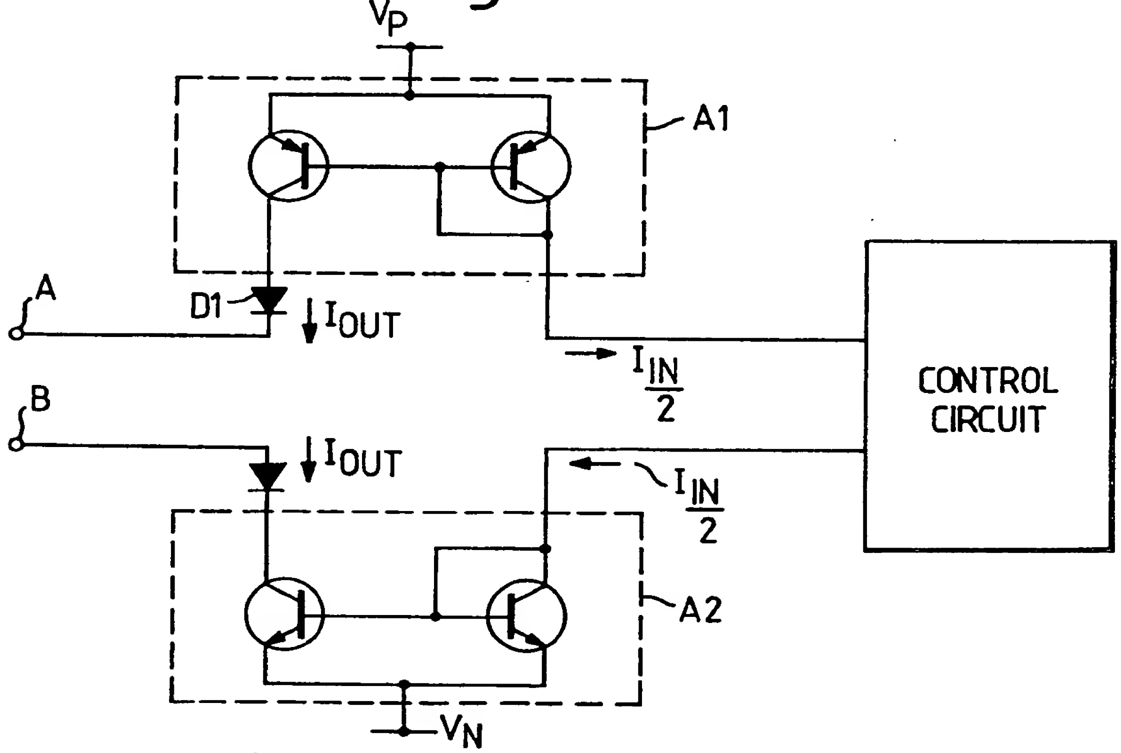
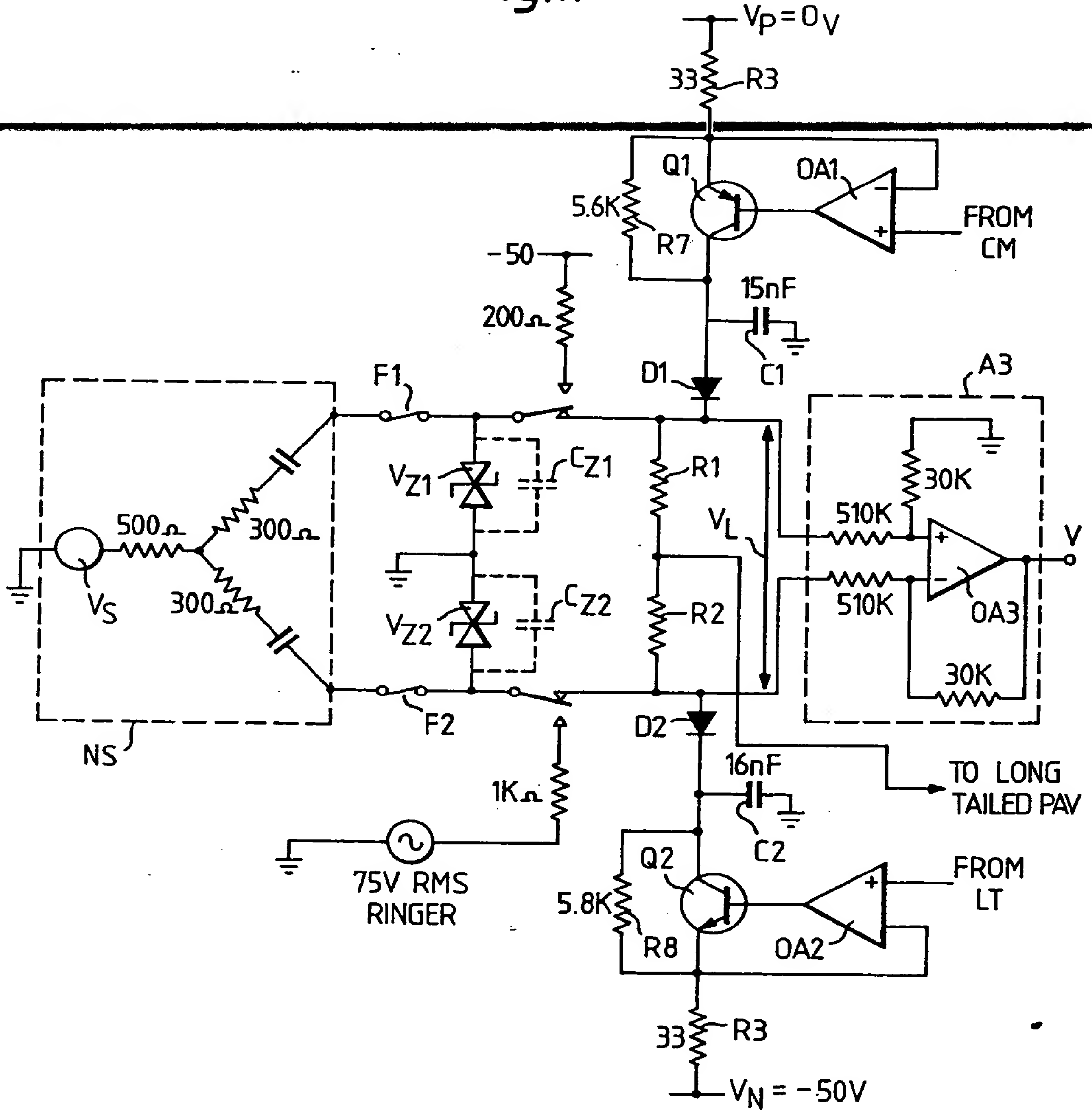

VP
A1
A
D1
IOUT
IIN/2
CONTROL CIRCUIT
B
IOUT
IIN/2
A2
VN

Fig.7.



VP=0V
33
R3
Q1
OA1
5.6K
R7
FROM CM
-50
15nF
200Ω
C1
D1
A3
F1
CZ1
VZ1
R1
30K
510K
VL
V
500Ω
300Ω
VS
300Ω
CZ2
VZ2
R2
510K
OA3
30K
NS
F2
D2
16nF
TO LONG TAILED PAV
1KΩ
C2
Q2
FROM LT
75V RMS RINGER
5.8K
R8
OA2
33
R3
VN=-50V

Fig.8.

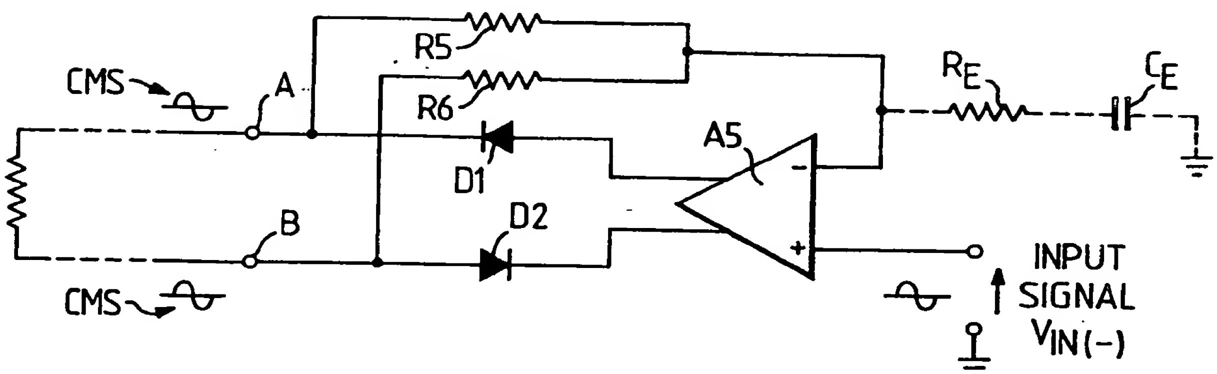


Fig.9.

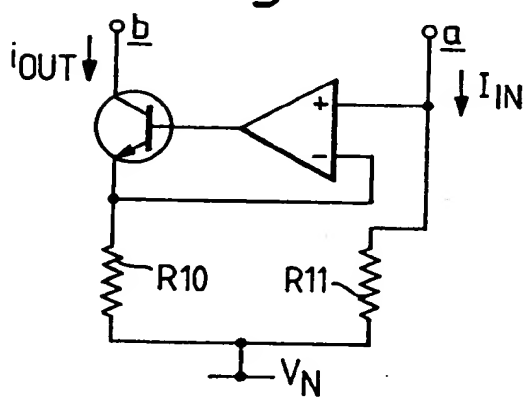


Fig.10.

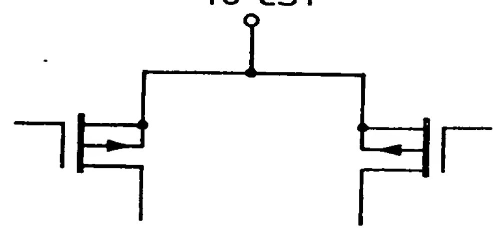


Fig.11.

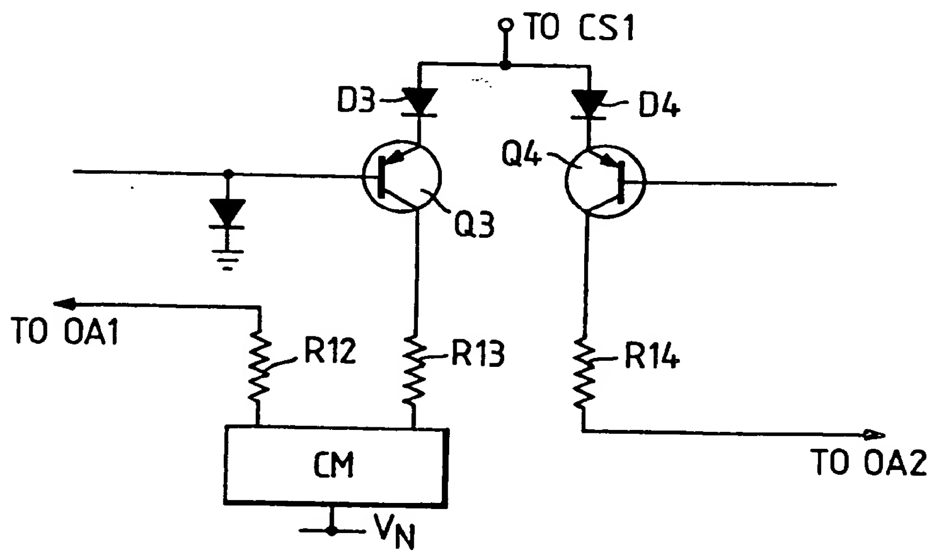


Fig.12.

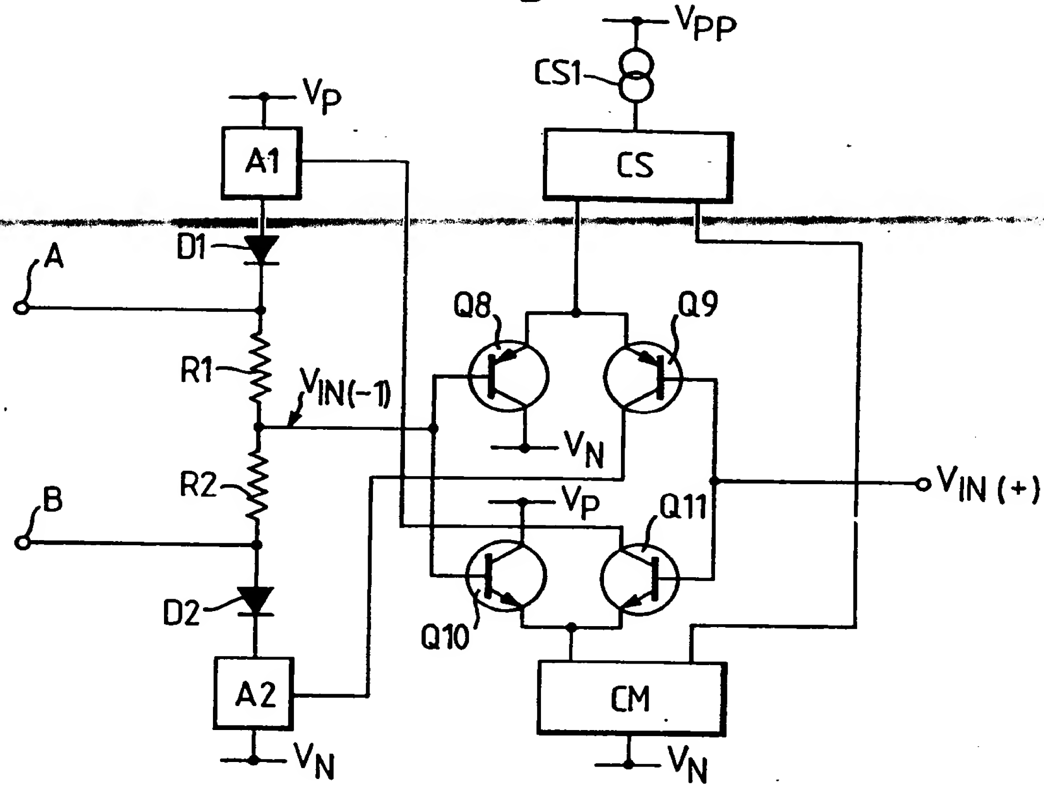

VPP
CS1
VP
A1
CS
D1
A
Q8
Q9
R1
VIN(-1)
VN
R2
VP
Q11
VIN (+)
B
D2
Q10
A2
CM
VN
VN

Fig.13.

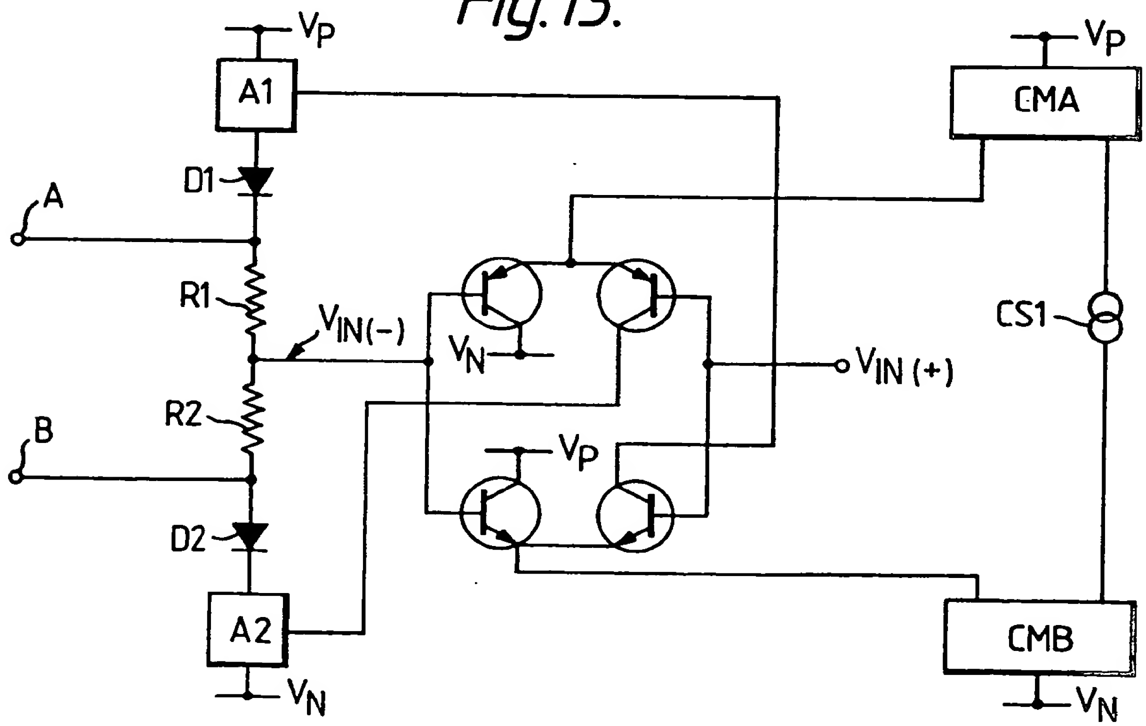

VP
A1
VP
CMA
D1
A
R1
VIN(-)
VN
VIN (+)
CS1
R2
VP
B
D2
A2
CMB
VN
VN

Fig.14.

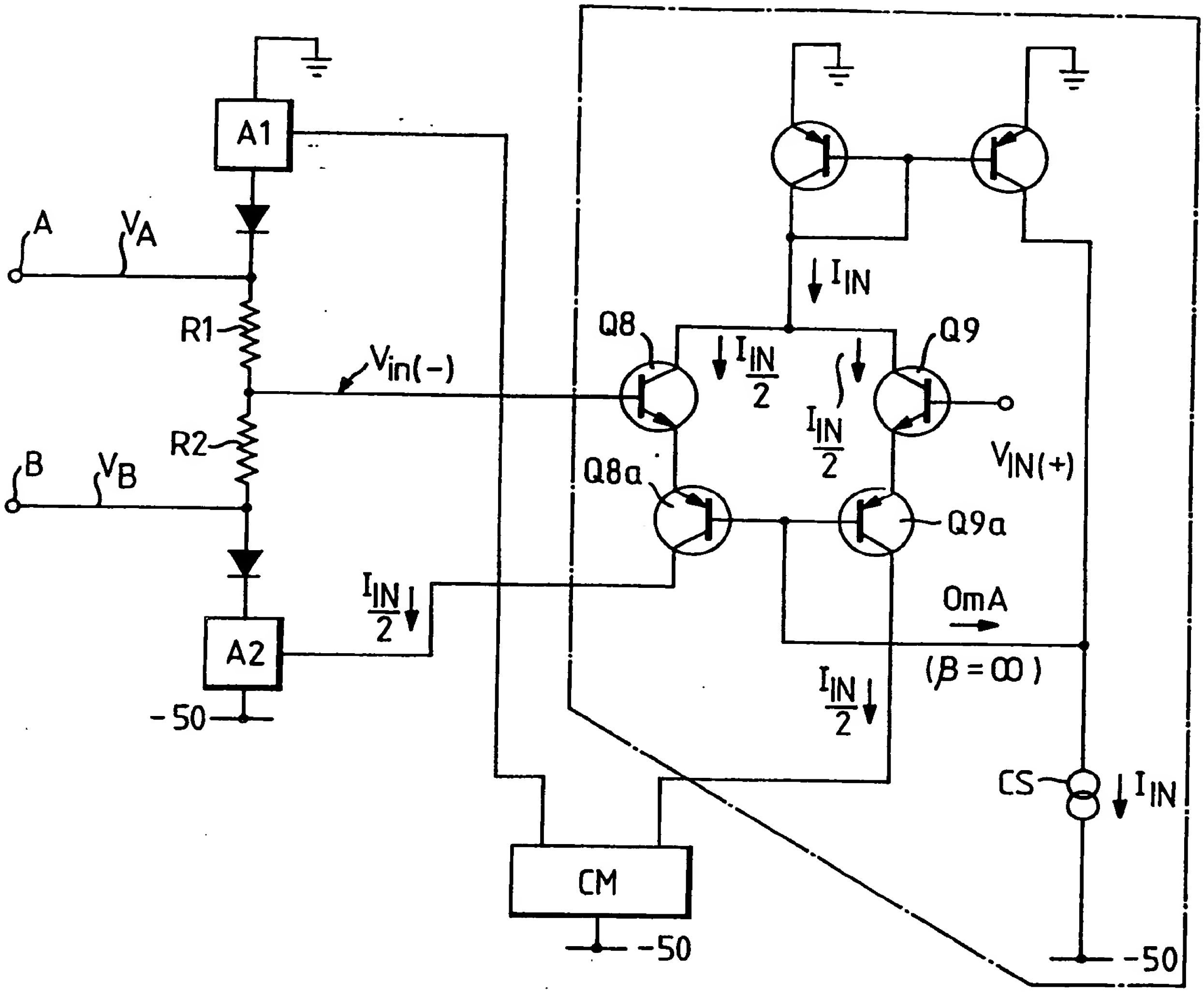

A1
A
VA
R1
Vin(-)
R2
B
VB
A2
-50
IIN/2
Q8
Q9
IIN
IIN/2
Q8a
Q9a
VIN(+)
0mA
(β=∞)
CS
-50
CM
-50

Fig.15.

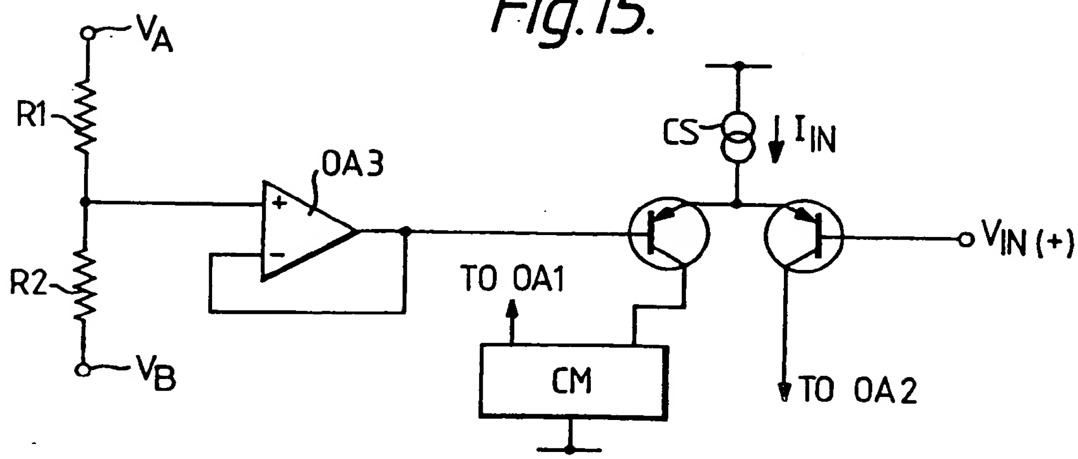
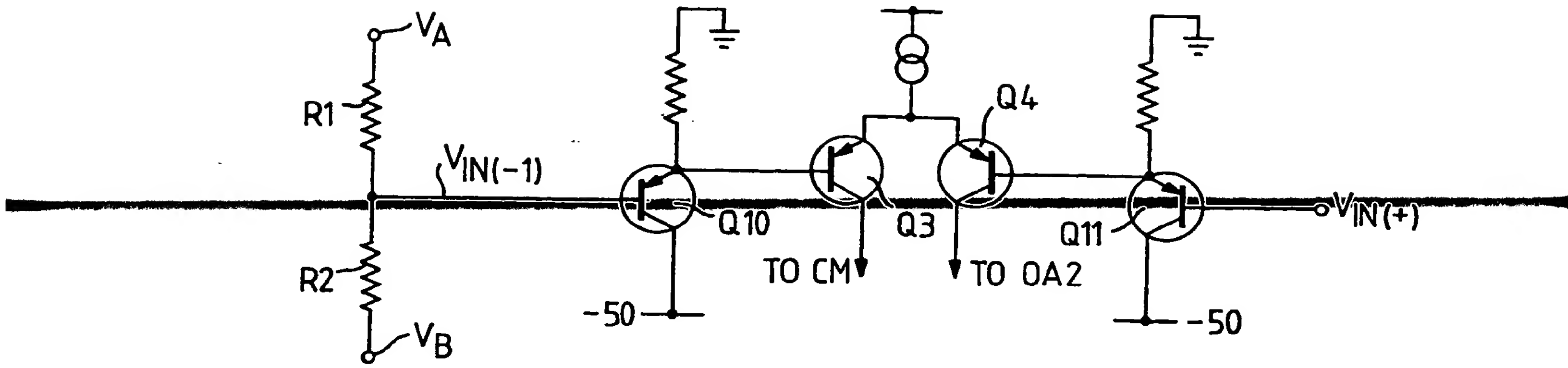
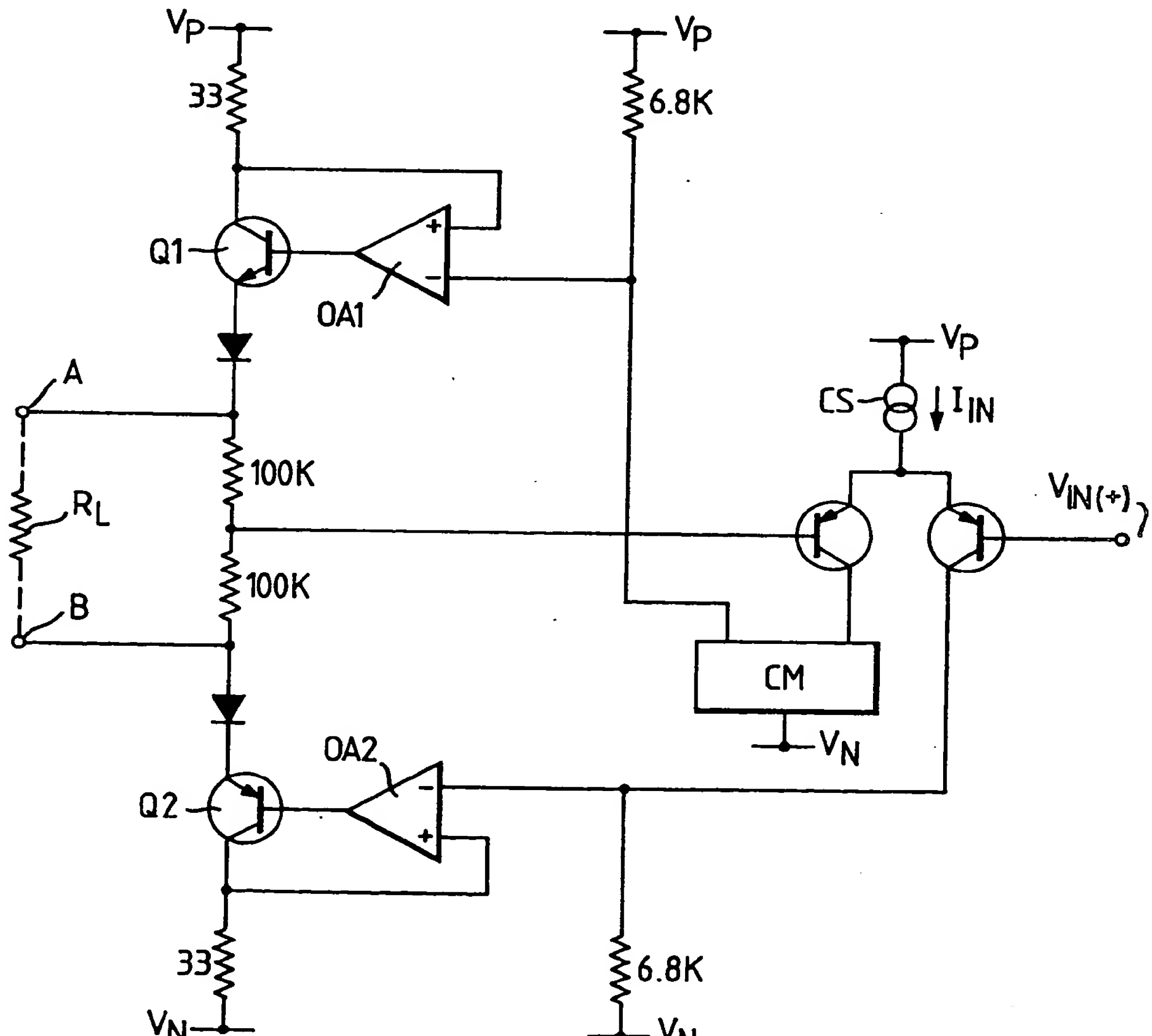

VA
R1
R2
VB
OA3
CS
IIN
VIN(+)
TO OA1
CM
TO OA2

Fig.16.



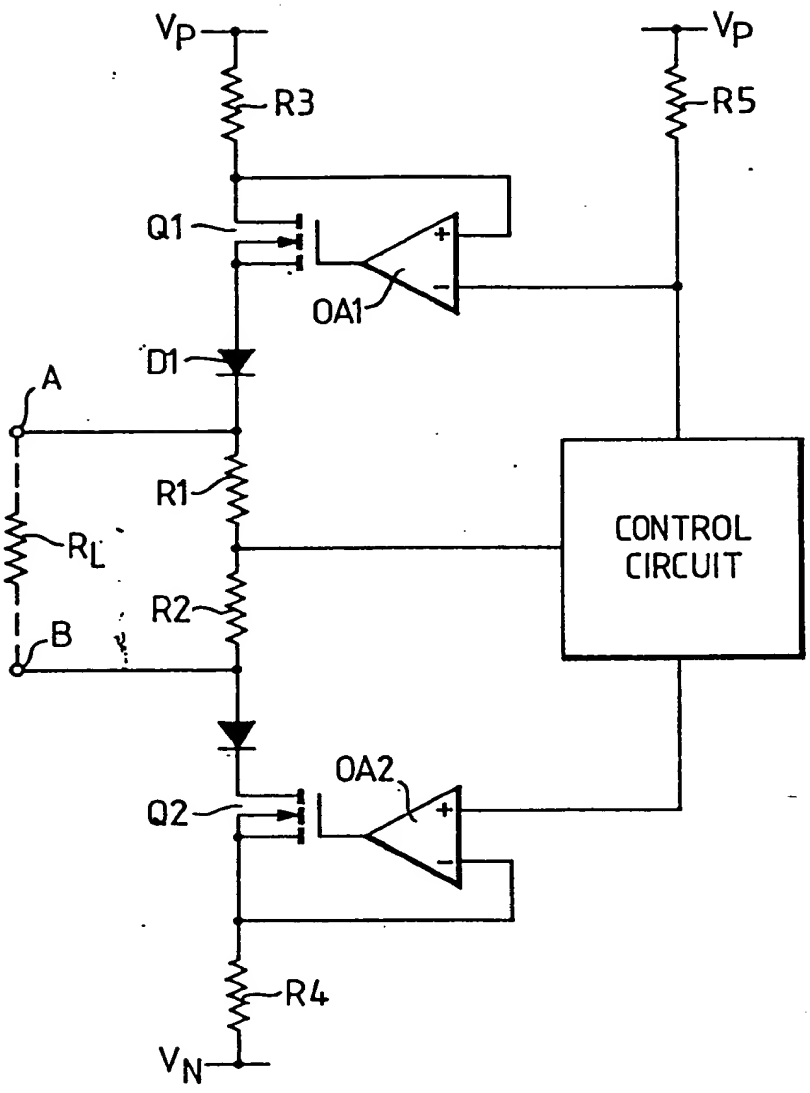
VA
R1
VIN(-1)
R2
VB
Q10
-50
Q3
TO CM
Q4
TO OA2
Q11
-50
VIN(+)

Fig.17.



VP
33
Q1
OA1
VP
6.8K
A
100K
RL
100K
B
VP
CS
IIN
VIN(+)
CM
VN
OA2
Q2
33
VN
6.8K
VN

Fig. 18.



SPECIFICATION

Telephone subscribers' line interface circuit

This invention relates to current feeding arrangements for telephone lines.

In the majority of telephone exchanges, the supply of current for the lines and the subscribers' apparatus connected thereto, is from the exchange via the line circuit at the exchange. It is desirable for the supply circuitry to be economical and also of high stability, and it is an object of the invention to provide line feed circuitry which satisfies these criteria.

According to the invention, there is provided a line feed amplifier for feeding the line current to a telephone line circuit, which includes a first current feed device connected between the more positive power supply terminal and a first leg of the line, a second current feed device connected between the more negative power supply terminal and a second leg of the line, a current source which supplies current to a control circuit for the current feed devices, a first connection from the control circuit via which the current supplied by the first current feed device is controlled, a second connection from the control circuit via which the current supplied by the second current feed device is controlled, a third connection from the control circuit to a point at a reference potential the value of which depends on the desired operating condition for the line to which the amplifier is connected, and a fourth connection from the line via which a potential whose value depends on the actual line operating condition is applied to the control circuit, the arrangement being such that variations in line operating conditions cause, due to comparator action in the control circuit, variations in the currents supplied via said connections to the current feed devices which variations control the current feed devices to adjust the line currents such that the desired line operating conditions are restored or maintained.

In the telephone exchange application, such an amplifier is used to supply direct current to a line to a telephone subscriber's premises. This direct current may be modulated with outgoing speech, so that in effect the result is an AC/DC source.

Embodiments of the invention will now be described with reference to the accompanying drawings, in which:

Figure 1 is a simplified circuit diagram of a first line feed circuit embodying the invention.

Figure 2 is an explanatory diagram derived from Figure 1, useful in explaining the invention.

Figure 3 shows the circuit of Figure 1 in more detail.

Figure 4 is a version of Figure 1 in which the transistor of the long-tailed pair are of the opposite conductivity to those of Figure 1.

Figure 5 is a circuit generally similar to part of Figure 1, but in which Q2 is a MOSFET. Q1 is also a MOSFET.

Figure 6 is a partial representation of a circuit which is generally similar to Figure 1, except that Q1—OA1 and Q2—OA2 are replaced by current mirrors.

Figure 7 shows how the line condition across the legs is sensed for control purposes such as line loop monitoring.

Figure 8 is a further explanatory diagram derived from Figure 1.

Figures 9, 10 and 11 show various alternatives for parts of Figure 1.

Figures 12 and 13 show alternative control structures to that of Figure 1.

The circuit shown in Figure 1 is a line feed amplifier arrangement for supplying a balanced current to the A and B legs of a telephone line which extends from the line circuit at the exchange to the subscriber's premises. This, when a call is set up for that line, is often modulated with speech, i.e. AC outgoing to that line. The resistance of the loop plus the subscriber's apparatus is represented by the resistor R_L while the current generators i_a and i_b represent induced common mode currents from disturbing sources. The arrangement supplies a current in one sense to one leg A and a current in the other sense to leg B of the line. The exchange DC supply is assumed to be 50 volts, with its positive side earthed to avoid electrolytic corrosion effects.

The line feed for the A, or positive leg is via a current feed device including a PNP transistor Q1 and an operational amplifier OA1 from which current flows to the A leg via a diode D1. For the B, or negative, leg there is another current feed device including an NPN transistor Q2 and operational amplifier OA2, connected to the line via a diode D2. This Q2—OA2 combination is similar to, but complementary to, Q1—OA1.

Connected across the line we have two equal-value high value resistors R1 and R2, the negative feed V_A and V_B for the voltage comparison function to be described below. Under normal operating conditions, the potential at the junction of R1 and R2 is —25 volts; this junction is connected to the base of a PNP transistor Q3, which is part of a long-tailed pair of Q3—Q4, which is a current splitter which performs a comparator function. The connection to the base of Q3 provides longitudinal negative feedback for the circuit. The current supply for Q3—Q4 is from a current source CS1 connected via diodes D3 and D4 to the (commoned) emitters of Q3 and Q4. The current source CS1 supplies the direct current from which the supply to the two legs of the loop is derived. It can be modulated with speech or other AC signals to be sent to the line for feeding the line differentially. Thus, it is in effect a combination of a DC source and an AC source, although its output is unidirectional. In one arrangement the source CS1 uses the output side of a long-tailed pair. However, it could use a circuit similar to OA1—Q1, and CS1 can be a current controlled source or a voltage controlled source. It could use two or more separate current sources in parallel.

The transistors Q3 and Q4 are similar, so their collector currents are equal, each such collector

current being equal to, or very close to, half the current from CS1. The base of Q4 is connected to a reference potential, which in this case is —25 volts.

Since the potential applied to the base of Q4 is a —25 volt reference, while that applied to the base of Q3 is the potential at the junction of R1 and R2, which should be —25 volts, the current flow in Q3 and Q4 depends on the relation between those two potentials.

The collector output of Q4 feeds an input current to a resistor R6, thus generating a defined input voltage for the non-inverting input of OA2, which compares its input voltage across R6 with the voltage across the resistor R4. OA2 adjusts its output voltage to make $V_{R6}=V_{R4}$. Thus OA2 effectively compares the current in the feed to the negative (B) leg of the line with the current due to Q4, and via the connection from its output to the base of Q2 it adjusts the value of the current in the negative leg. The current in the collector circuit of Q3 exercises a similar control on the feed to the other (A) leg of the line via a current mirror CM. A current mirror is used here in view of the different voltage levels to be applied to the two legs. CM can be said to "bounce" the signal back up to the top "rail" of the DC supply.

Thus we have a differential voltage stimulus applied to the emitters of Q3 and Q4 from CS1, via diodes D3 and D4, and this appears in the collector circuits of Q3 and Q4 in the same sense. From there it is applied via OA2—Q2 to the B leg, where it is inverted as compared with its polarity at the input to OA2.

The negative feed back conditions and the common mode voltage sensing will now be discussed. The common mode voltage is sensed on both legs of the line, and is assumed to be positive-going. This opposes the differential voltage stimulus in the collector of Q1, the base of Q1 and on the non-inverting input of OA1. It also has an effect on the base of Q3, due to the connection thereof to the junction of R1 and R2. In addition, via the current mirror CM, this common mode voltage sensing also influences the collector circuit of Q3 in a sense opposed to the effect of this differential voltage stimulus. The common mode voltage sensed on the B leg, opposes the differential voltage stimulus in the collector of Q2, the base of Q2 and on the non-inverting input of OA2, and hence on the collector of Q4.

Thus variations in the line current which vary the voltage at the junction of R1—R2 cause due to the comparator action of Q3—Q4, a correction which causes the line to tend to remain balanced. Hence the current source CS1 controls the transverse circuit (see below), while the reference potential applied to the base of Q4 controls the longitudinal circuit. The transverse circuit is significant for speech feed as speech (and any other AC signal) is modulated onto the DC from CS1. One of the two operational amplifiers OA1 and OA2 has a fast slew rate (see below), in this case OA1.

Thus the same current source CS1 does two jobs, firstly to control the steady state loop current according to the feed law needed and secondly to control the instantaneous loop current due to transmitted speech.

We now refer to Figure 2, which is intended to indicate schematically the various functions of Figure 1, the same references being used when possible. These functions are:

(a) The loop current linear control for both AC and DC is exercised by the current source CS1.

(b) The voltage comparison function for both AC and DC is indicated by the broken line VC; this is independent of the linear control, item (a).

(c) Broken line OAF indicates the output amplifier DC and AC voltage rejection functions.

(d) The blocks A1 and A2, corresponding to Q1—OA1 and Q2—OA2 respectively, represent the current gain function, and are equivalent to 2K resistors.

(e) R1 and R2 do the voltage sensing function and their common point performs an addition function.

(f) The differential voltage sensing function is effected from across R_L, and is schematically indicated at A4. The current in R_L is $I_L=KI_{IN}$.

(g) Another comparison function is indicated by the block COMP, for the system control function associated with the line circuit.

The voltage $V_{IN(+)}$ is the desired line condition reference voltage, both for DC and AC, and it will be seen that a first negative feedback loop extends from the junction of R1 and R2 to supply $V_{IN(-)}$ to the control circuit. A second negative feedback loop extends to CS1, as indicated. The voltage

$$\frac{V_A+V_B}{2}$$

is the common mode line condition sum signal, which influences the currents supplied to the line under control of the control circuits (Q3—Q4, etc., Figure 1) H_A and H_B represent internal and external heat rejection functions.

The following are unwanted input signals, as "seen" at A and B, which have to be rejected:

V_P=Positive power supply (DC and AC signals)
V_N=Negative power supply (DC and AC signals)
$\left.\begin{array}{l}H_A=\\H_B=\end{array}\right\}$ Self heating signals and heat signals from external sources.
$\left.\begin{array}{l}i_A=\\i_B=\end{array}\right\}$ Induced common mode currents from disturbing sources.

To explain the functions, we group them under four headings,

(a) Voltage comparator function (DC and AC) and Common Mode Line Voltage Function (Balance)

The Control Circuit provides a voltage comparator function between inputs $V_{IN(-)}$ and

$V_{IN(+)}$. This comparator has two outputs which can drive the legs of the balanced line via current amplifiers. The comparator is connected within the common mode negative feedback loop OAF. Thus it compares the common mode line condition with a desired line condition, a DC or AC reference signal, and adjusts the common mode output line voltage to be equal to the reference voltage.

When operation is linear, the loop maintains balance by applying a correction from the comparator against disturbing influences such as mismatched components and externally induced common mode currents in the line. One result of the negative feedback is a low common mode output impedance, but the differential output impedance remains high. The common mode line condition signal feedback for comparison can be attenuated to give a common mode closed loop voltage gain greater than unity, i.e. the DC or AC voltage reference signal is amplified on to the line.

(b) Loop Current Linear Control Function (AC and DC) Differential Circuit

The loop current I_L, i.e. the output of the differential circuit, is controlled by the linear control input signal I_{IN} from CS1. This function operates independently of the first discussed function under linear condition, according to orthogonal control principle. I_L is controlled only by I_{IN}, because I_L is independent of power supply voltages and is also independent of self generated and externally generated heat signals. Also I_L is independent of R_L and of the common mode circuit.

The differential circuit works linearly down to zero DC, i.e. to $I_{IN}=0$, under linear operating conditions, and the DC and AC signals are fed to the line differentially. The output current amplifiers A1 and A2, i.e. the current feed devices Q1—OA1 and Q2—OA2, provide current gain, with $I_L=K.I_{IN}$, where the current gain K may be as much as 100, and the DC and AC gains are equal.

Negative feedback is applied to the differential circuit independently of the common mode circuit, i.e. the linear control input is in a negative feedback loop responding to a feedback signal derived from the differential line condition. The input current source I_{IN} can itself be voltage or current controlled, and it can be grounded or floating, depending on the structure adopted for the control circuit. Only a single input is needed to control the loop current, but one can connect several current sources in parallel, so that the loop current linear control input forms a current summing junction for different input signals.

(c) Power Supply Voltage Rejection Function (DC and AC)

The circuit rejects direct and alternating voltages from the power supplies, i.e. the loop DC and AC are substantially unaffected by direct and alternating voltages from the power supplies V_P and V_N. The voltage rejection is provided in the control circuit and the output stages (A1 and A2), and is provided for the common mode circuit, but the most important voltage rejection is the differential circuit rejection. Thus I_L is independent of the supply voltages V_P and V_N.

This rejection prevents a differential noise signal from being injected into the two wire loop and the four-wire transmit path from V_P and V_N, i.e. battery noise rejection. This rejection also means that I_L (DC) is independent of the power supply direct voltages, as long as the circuit is also independent of the change to the self-heating due to changes in the power supply voltage—see (d), below.

Thus the line feed amplifier can operate as a true constant DC source I_L (DC) when fed by a constant input I_L (DC), so that I_L (DC) is independent of V_P and V_N and of R_L. The AC gain is also independent of the V_P and V_N.

Noise on the operational amplifier supply rails is also rejected by OA1 and OA2.

(d) Heat Rejection Function

Heat rejection is provided in the control circuit and the output stages (A1 and A2), and the loop current. I_L is substantially independent of internal and external heat signals. Thus I_L is independent of changes in self-heating due to changes in V_P and V_N, so the differential DC and AC gain is independent of temperature.

Thus the circuit embodies the above four functions simultaneously in combination, and they operate independently under linear conditions. It handles four dimensioned variables, common mode voltage, differential current, power supply voltage and heat signals.

In the more detailed circuit of Figure 3, many component values are shown. If the transistors, Q1 is an MJE 350, Q2 is a BUY 49P, Q3 and Q4 are MMBTA 93, and Q5 and Q6 are MMBTA 43. The last four are packaged in SOT 23 packages. OA1 is an LF 351A, and OA2 is half of an LM 358 unit. Z_T i the line termination, and in a complex CR network, connected in series with a high-value capacitor.

OA1 is a fast slew rate operational amplifier, its slew rate being of the order of 10 volts/sec, and it works off ±5 volts. Its input voltage V_{IN} is −1.32 volts, which is the current voltage across the 6.8K resistor due to the 200 A current from the transistor Q6 of the current mirror (CM in Figure 1). Similarly, OA2 has an input voltage of 1.32 volts, and its inputs must work down to 0.5 volts above the negative rail (−50V) and so OA2 consumes low power, so it has a slow slew rate.

Thus it will be seen that the line feed amplifier of Figure 1 includes output current generators Q1—OA1 and Q2—OA2 in which high power dissipation is permitted in the output transistors Q1, Q2, e.g. 1 watt per leg, and a control circuit whose power dissipation is low, e.g. 30 mW. The loop resistance is the total DC resistance of the two wire line in series with the resistance of the subscriber's telephone.

Note that many different sorts of current

mirrors other than that shown can be used instead of the Q5—Q6 arrangement shown.

In Figure 2, $V_{IN(+)}$ is derived by the potential divider formed by two 470K resistors. The resultant voltage is decoupled to AC by the capacitor C_D, which prevents noise on the power supply V_N appearing at $V_{IN(+)}$ and so being fed onto the line as a common mode AC noise voltage. Variations in direct voltage automatically adjust the circuit so it is balanced about the mid-point of the power supply direct voltages.

Figure 4 shows a similar circuit structure to that shown in Figure 1 but with the polarity of the control circuit transistors reversed. Here the blocks A1 and A2 represent Q1—OA1 and Q2—OA2 respectively.

The output stages Q1—OA1 and Q2—OA2 (Figure 1) are single-ended current generators which provide unidirectional current flow to the line, the series output resistors R3 and R4 being grounded, at least for AC. Further the low value resistors R3, R4, in this case 33 ohms, give minimum series voltage drop. They also maximise line length possible for a given current and battery voltage. They also give loss power dissipation. The output transistors Q1 and Q2 dissipate the feed power and provide high voltage isolation since overvoltage detectors (not shown) switch them off. Since each leg has an independent local negative feedback loop, the line current is substantially independent of the V_{BE} of Q1 and Q2. Thus the circuit is not affected by the values or tolerances of V_{BE}, or of their variation with transistor junction temperature. This improves line current tolerance and eliminates line current variations with temperature due to:

(a) variation of power dissipation with line length and battery voltage; which cause self-heating of Q1 and Q2.

(b) heat coupling to Q1 or Q2 from other line driver transistors when using a shared heat sink.

(c) warm up drift in Q1 or Q2 after going off hook.

(d) ambient temperature variation.

The output stages can drive either bipolar transistors, or MOSFETS, as shown in Figure 5 for the B leg. Here Q2 is an N-channel MOSFET, which eliminates h_{FE}, thus reducing the emitter-to-collector current loss compared that for a bipolar transistor. Note that a P-channel MOSFET is needed on the A leg. As compared with the circuits using bipolar transistors OA1 and OA2 need to have sufficiently large power supply voltages to drive the larger output voltaged needed for MOSFETS. Thus instead of —5V supply to OA1 as in Figure 1, we need —10V.

In Figure 1, the output stages operate in a manner similar to current mirrors with high current gain, e.g. 200, facilitating the use of a low power control circuit. The complementary differential output is symmetrical to both DC and AC signals.

In Figure 6, A1 and A2 show high gain current mirror output amplifiers as the current feed devices for the two legs.

The structure of the basic circuit of Figure 1 can be regarded as two amplifiers superimposed at right angles, i.e. a differential current amplifier supplying current $K.I_{IN}$ to the A and B legs, and a common mode voltage amplifier supplying $V_{IN(+)}$ to the mid-point of the A and B legs. Here $V_{IN(+)}$ is the non-inverting input and $V_{IN(-)}$ is the inverting input of the common mode amplifier. These amplifiers have common outputs, the A and B legs, but separate inputs, I_{IN} and $V_{IN(+)}/V_{IN(-)}$, and they operate independently in the linear region. Note that $I_L=K.I_{IN}$, so if $K=100$ and $I_{IN}=0.4$ mA, we have $I_L=40$ mA. Thus their characteristics are independently adjustable by separate negative feed back loops and separate components.

A single low level current source CS1, which supplies I_{IN}, controls the loop current in both legs of the differential output, and a single voltage source $V_{IN(+)}$ (the reference voltage on the base of Q4) controls the common mode output voltage. The long-tailed pair Q3—Q4 splits the control current I_{IN}, directing part to the B leg current drive circuit Q2—OA2, and part to the current mirror CM to provide voltage phase reversal and the drive current for Q1—OA1 for the A leg. Thus the long-tailed pair acts as a current splitter.

The common mode negative feed back loop from the differential outputs to the inverting input $V_{IN(-)}$ (base of Q3) forces the outputs to be automatically balanced about $V_{IN(+)}$ when R1=R2 because the virtual earth thus applied to Q3—Q4 holds $V_{IN(-)}$ close to $V_{IN(+)}$. If $V_{IN(+)}$ is equal to the voltage at the mid-point of the power supplies V_P and V_N, the outputs are balanced about this mid-point voltage. This negative feedback also sets up a low common mode output impedance, e.g. 30 ohms in a practical stable circuit, while the differential output impedance remains high. This output impedance "sinks" externally-induced common mode currents flowing into the A and B leg outputs, so only a small voltage drop is added to the common mode output voltage. The line currents I_A and I_B vary in sympathy with the induced common mode current, while the loop current I_L remains constant, determined by I_{IN}. The maximum line current can swing up to 2 I_L in one leg, while the current in the other leg can swing down to zero. Thus the arrangement maintains a low common mode impedance when the peak common mode current is less than the loop DC. Further, the maximum common mode current limit for linear operation (low impedance) decreases as loop current I_L decreases, so the following low loop current conditions need consideration:—

(i) unlooped idle lines, when $I_L=0$

(ii) during dialled pulse breaks, when I_L degrades towards zero

(iii) idle line battery charging, when (in one case) $I_L=4$ mA

(iv) out of limit lines, when $I_L<25$ mA when normally looped.

At low loop currents, a positive-going common

mode voltage swing switches the current off in the A leg and switches it to a maximum constant level $2I_L$ in the B leg. Conversely a negative swing switches the B leg off and switches the A leg to a constant level $2I_L$. The amplifier has a high common mode output impedance in these two non-linear switched states because the line driver transistor on one leg Q1 or Q2 is a high impedance constant current source supplying $2I_L$ (I_L=0 on an unlooped line is a special case), and the series protection diode D2 or D1 is cut off on the opposite leg.

As the common mode voltage swings from one non-linear state to the other, it passes through a transitional linear state in which it has a low common mode impedance, dependent on the loop current value I_L.

On unlooped idle lines there is negligible distortion of the common mode waveform because I_L=0, whereas due to the break pulse in loop disconnect dialling there are linear, variable non-linear, and variable transitional states as the loop current discharges from a high value towards zero and charges up to a high value again. The high common mode output impedance in the non-linear state allows the full common mode induced source voltage to be developed on both legs of the circuit, e.g. 50 volts peak to peak, so the common mode voltage waveform swings the A leg above the V_P rail voltage, and swings the B leg below the V_N rail. We now refer to Figure 7, which shows part of Figure 1, with some additional components. From the above description it will be seen that secondary protection voltage clamping devices V_{Z1} and V_{Z2} connected across the line and to earth, need sufficient stand-off voltage to prevent severe clipping distortion of the common mode waveform when loop current is low. Further, a differential voltage sensing amplifier A3 connected to the A and B legs for feed law synthesis and loop detection etc. must operate correctly with its inputs outside the V_P/V_N rails to reject the common mode signal on idle lines and during dialling etc.

Line wetting resistors R7 and R8 are shown in Figure 7 for these:—

(i) To provide a "wetting" voltage on an idle line
(ii) To provide DC bias for park detection
(iii) To reduce power dissipation in Q1 and Q2
(iv) To give overvoltage detection, and
(v) To lower the common mode output impedance when D1 and/or D2 are forward biased in the non-linear state.

In the linear mode, R7 and R8 look open-circuit to line signals due to the local negative feedback loops around OA1 and OA2. Similarly, the output transistor r_{CE} of Q1 and Q2 is eliminated by the virtual earth summing point on the emitters of Q1 and Q2, which gives a high differential output impedance.

The imbalance due to the differences in the offstate capacitances C_{Z1} and C_{Z2} of protection devices is reduced by capacitors C1 and C2, which also stabilise the common mode negative feedback loop in the linear mode. In one case C1 and C2 have values of 15 nF and 16 nF respectively. Another stability requirement is that OA1 or OA2 must (as already mentioned) be a high slew rate operational amplifier, e.g. 10V/μs, to avoid instability of the feedback loop by slew rate limiting.

The series diodes D1 and D2 protect the line driver transistors Q1 and Q2 and the driver operational amplifiers OA1 and OA2 against positive overvoltage on the A leg and negative overvoltage on the B leg. They also allow a high common mode output impedance at low loop currents (as described above). D1 and D2 are *inside* the common mode negative feedback loop so that in the linear mode the negative feedback overcomes the imbalance of mismatched diode voltage drops, and reduces the effect of the diode slope resistance on the low common mode output impedance at low loop current. In general, the negative feedback overcomes the imbalance of any mismatched series elements, e.g. positive temperature coefficients devices or poly-switches, which are inside the feedback loop.

In Figure 7, the elements in the dashed box NS represent an externally induced common mode voltage source, assumed to correspond to a 20 volt RMS source. The elements F1 and F2 are fuses, each having a resistance of 22.5 ohms. V_{Z1} has a ± 65 volt stand-off, and V_{Z2} has a ±130 volt stand-off.

The box A3 contains a differential voltage sensing amplifier whose inputs work outside the V_P and V_N rail voltages. The output voltage $V_{OUT}=V_{L/17}$, as can be seen from the values of the resistors connected to OA3. This indicates to the exchange equipment the line condition.

The common mode circuit, Figure 1, is structured as a voltage follower with unity voltage gain. If the feedback signal is attenuated by an additional shunt impedance R_E in the feedback path, see Figure 8, the voltage gain is increased. Only the AC gain is increased if a blocking capacitor C_E is in series with R_E. The increased gain increases the common mode output impedance.

In Figure 8, CMS represent common mode signals generated by the amplifier in response to an input signal applied to $V_{IN(+)}$, and A5 represents the common mode voltage amplifier Q3/Q4—A1/A2.

Common mode AC and DC signals can be fed to line, see Figure 3, by applying an input signal to either $V_{IN(+)}$ or $V_{IN(-)}$. The common mode output voltage is limited by the Q1 and Q2 "headroom" and the current limited by I_{IN}. The voltage "headroom" decreases with increasing line length so only small signals can be generated on long lines. The power supply voltages V_P and V_N need to be increased to generate large undistorted common mode signals on the long lines.

It is important to note that the feed amplifier structure inherently rejects noise on the power supplies V_P and V_N because:—

(i) Input I_{IN} from CS1 rejects power supply noise.
(ii) Long-tailed pair current source high impedance outputs reject power supply noise.
(iii) Current mirror (CM) floats on top of power supply noise.
(iv) Output current amplifiers A1 and A2 (i.e. Q1—OA1 and Q2—OA2) float on power supply noise. Hence no differential noise signal is injected into the two-wire loop, and no noise signal is injected into the four wire transmit path (not shown), extending into the exchange. In telephone parlance, this is often called battery noise rejection as noisy battery supplies are often used to power the circuits (e.g. V_P=0V, V_N=50V) OA1 and OA2 also reject noise from their supplies.

The unity gain current mirror in Figure 1 can use discrete or integrated circuit transistors, or may use an operational amplifier circuit as shown in Figure 9 if the delay through the operational amplifier in Figure 9, is not excessively long, otherwise it could cause the overall circuit of Figure 1 to oscillate. It thus replaces CM in Figure 1, with *b* connected to OA1 and *a* to the collector of Q3. The current ratio is thus

$$\frac{i_{OUT}}{i_{IN}} = \frac{R11}{R10}$$

VMOS input transistors can be used, see Figure 10, and they eliminate the emitter to collector current loss of the long-tailed pair, and also reduce output offset due to base current generated voltage drop in R1/R2 (Figure 1). When the arrangement of Figure 10 is used, its common point goes to the current source CS1. Such an arrangement can also use JFETs.

The long-tailed pair transistors Q3 and Q4 are protected by the emitter dioides D3 and D4, see Figure 11. Further, D3 prevents an earth on the base of Q3 from forcing a large current via Q4 into the input of the output amplifier Q2—OA2, which would otherwise generate a large output current resulting in overdissipation in Q2. R12, R13 and R14, all of 6.8K, drop unwanted voltage in the control circuit without affecting the circuit operation.

Figure 12 shows an alternative control structure in which the controlling long-tailed pair of Figure 1 is replaced by complementary pairs Q8—Q9 and Q8a—Q9a. These are so connected that their base currents cancel each other, reducing the base current generated voltage drop in R1 and R2. Here CS represents a circuit such as a current mirror connected as a current splitter, so that half the current from the CS1 goes to Q8—Q9 emitters, and half goes to the current mirror CM. The current mirror has unity current ratio if the current splitters' output currents are equal.

A1 corresponds to Q1—OA1 of Figure 1, driven from the collector of Q11, while A2 corresponds to Q2—OA2 of Figure 1, driven from the collector of Q9.

The circuit of Figure 13 is generally similar to that of Figure 12, except that instead of using a current splitter and a current mirror, it uses two current mirrors CMA and CMB with the current source CS1 connected between them. CMA and CMB have unity current ratios or equal current gains.

The current splitter CS in Figure 12 allows the CS1 to be grounded, unlike that of Figure 13, and results in only $I_{IN/4}$ reaching A1 and A2, unless the current splitter has current gain (I_{IN} is the current from CS1).

Another method to reduce the base current generated voltage drop in R1 and R2 (Figure 1) is to add a buffer operational amplifier (high input impedance) or to add emitter follower input buffers, see below.

In an integrated circuit realization of the circuit it might be desirable to use a pseudo long-tailed pair control circuit, as will be seen (see below), since high current gain PNP input transistors are difficult to achieve in some integrated circuit technologies. In this case, the output connections are changed over due to the different phase relationships between inputs and outputs.

Figure 14 shows a circuit derived from Figure 1, in which, for convenience of realization in integrated circuit form the control circuit is a pseudo long-tailed pair which is similar to that used in the 741 operational amplifier. This, which uses NPN transistors, is the equivalent of the ordinary long-tailed pair with PNP transistors, as used in Figures 1 and 3. Since the circuit is based on NPN, and not PNP transistors, in this case it is current feed device A1(Q1—OA1), which is controlled via the current mirror CM, and not A2 (Q2—OA2) as in Figure 1.

In this circuit I_{IN} is once again, in the telephone application, the DC supply which may be modulated with outgoing speech or other signals.

Such a circuit has the advantage that with an integrated circuit realization high gain NPN transistors are in some cases easier to realise than high gain PNP transistors.

Another method of reducing the base-current generated voltage drop in R1 and R2 (Figure 1) is to add a high input impedance operational amplifier buffer OA3 as shown in Figure 15, or emitter follower buffers in the connections to the bases of the long-tailed pair transistors as shown in Figure 16. In this circuit it is preferable, although not shown, for the −50 volt supply to these emitter followers Q10 and Q11 to be filtered to attenuate battery noise.

Figure 17 shows an alternative arrangement for the current feed devices of Figure 1, in which Q1 is an NPN transistor, whereas in Figure 1 it is a PNP, while Q2 is a PNP, and not an NPN as in Figure 1. Thus Q1 and Q2 are connected as emitter followers instead of in the grounded emitter configuration as in Figure 1. Thus the input connections to OA1 and OA2 are reversed because in this case the phase inversion for the negative feedback loop around Q1—OA1 or Q2—

OA2 is supplied by Q1 or Q2 and not OA1 or OA2. These amplifiers OA1 and OA2 in this case have higher output voltages than for Figure 1. Series output resistors are grounded.

Figure 18 is another circuit derived from Figure 1, but in which the transistors Q1, Q2 are replaced by N-channel MOSFETs G1 and G2. Note that complementary MOSFETs are not needed. Series output resistors are grounded.

Suitable alteration of connection enables P-channel MOSFETs to be used.

Claims

1. A line feed amplifier for feeding the line current to a telephone line circuit, which includes a first current feed device connected between the more positive power supply terminal and a first leg of the line, a second current feed device connected between the more negative power supply terminal and a second leg of the line, a current source which supplies current to a control circuit for the current feed devices, a first connection from the control circuit via which the current supplied by the first current feed device is controlled, a second connection from the control circuit via which the current supplied by the second current feed device is controlled, a third connection from the control circuit to a point at a reference potential the value of which depends on the desired operating condition for the line to which the amplifier is connected, and a fourth connection from the line via which a potential whose value depends on the actual line operating condition is applied to the control circuit, the arrangement being such that variations in line operating conditions cause, due to comparator action in the control circuit, variations in the current supplied via said connections to the current feed devices, which variations control the current feed devices to adjust the line current such that the desired line operating conditions are restored or maintained.

2. An amplifier as claimed in claim 1, in which the control circuit includes a long-tailed pair the transistors of which have their emitters connected together and to the current source, in which the collector of one of said transistor is connected to the second of said current feed devices, in which the collector of the other of said transistor is connected to the input of a current mirror circuit, and in which the output of said current mirror circuit is connected to the first of said current feed devices.

3. A circuit as claimed in claim 2, in which the base of said one of the transistors is connected to a point at a reference potential, in which two resistive impedances of the same value are connected in series between the two legs of the line, and in which the junction point of the two resistive impedances is connected to the base of the other of said transistors, so that the comparator action is between the potential at the junction of the two resistive impedances and the reference potential.

4. A line feed amplifier for feeding the line current to a telephone line circuit, which includes a first current feed device connected between the more positive power supply terminal and a first leg of the line, a second current feed device connected between the more negative power supply terminal and a second leg of the line, a current source which supplies current to the commoned emitters of a long-tailed pair, a connection from the collector of one transistor of the long-tailed pair to the first of the current feed devices via which the collector current of that one transistor controls the current supplied via the first current feed device, a connection from the collector of the other transistor of the long-tailed pair to a first transistor of a current mirror via which the operation of that current mirror is controlled, a connection from another transistor of the current mirror to the second of the current feed devices via which the current supplied by that second current feed device is controlled, so that the second current feed device is controlled from the long-tailed pair via the current mirror, a connection from the base of one transistor of the long-tailed pair to a point at a reference potential whose value depends on the desired operating conditions of the line, and a connection from the line via which a potential whose value depends on the line operating condition is applied to the base of another transistor of the long-tailed pair, the arrangement being such that variations in line operating conditions cause, due to comparator action in the long-tailed pair, variations in the relative collector currents of the long-tailed pair transistors, which variations control the current feed devices to adjust the line currents, such that the desired line operating condition is restored or maintained.

5. An amplifier as claimed in claim 4, and which includes a diode in series with the emitter of each of the transistors of the long-tailed pairs.

6. An amplifier as claimed in claims 1, 2, 3, 4 or 5, in which two resistive impedances of the same value are connected in series across the line, the junction between said two resistive impedances supplying the said potential whose value depends on the line operating conditions.

7. An amplifier as claimed in claim 1 or 2, in which the control circuit includes two long-tailed pairs the second of which uses transistors of the opposite polarity type from those used by the first of these long-tailed pairs, in which the current source feeds a current splitter having two outputs the currents from which are equal, in which one of the outputs from the current splitter is connected to the commoned emitters of the first long-tailed pair and the other output of the current splitter is connected to the input of a current mirror, in which the base of the first transistor of the first long-tailed pair is connected to the base of the first transistor of the second long-tailed pair and to said potential whose value depends on the lines operating condition, so as to form said fourth connection, in which the base of the second transistor of the first long-tailed pair is connected to the base of the second transistor of the second

long-tailed pair and to the source of said reference potential, so as to form said third connection, in which the collector of one transistor of the first long-tailed pair is connected to one of said current feed devices, in which the collector of one of the transistors of the second long-tailed pair is connected to the other of said current feed devices, and in which the commoned emitters of the transistors of the second long-tailed pair are connected to the output of said current mirror.

8. An amplifier as claimed in claim 1 or 2, in which the control circuit includes two long-tailed pairs, the second of which uses transistors of the opposite polarity type from those used by the first of the long-tailed pairs, in which the current source is connected between the inputs of a first and second current mirror, in which the output of the first current mirror is connected to the commoned emitters of the first long-tailed pairs, in which the base of the first transistor of the first long-tailed pair is connected to the base of the first transistor of the second long-tailed pair and to said potential whose value depends on the line's operating conditions, so as to form said fourth connection, in which the base of the second transistor of the first long-tailed pair is connected to the base of the second transistor of the second long-tailed pair and to the source of said reference potential, so as to form said third connection, in which the collector of one of the transistors of the first long-tailed pair is connected to the second current feed device and the collector of one of the transistors of the second long-tailed pair is connected to the first current feed device, and in which the commoned emitters of the transistors of the second long-tailed pair are connected to the output of the other current mirror.

9. An amplifier as claimed in any one of the preceding claims and in which each said current feed device is connected to the leg of the line via a diode in its low resistance state for current from that device.

10. An amplifier as claimed in any one of claims 1 to 9, in which each said current feed device includes an operational amplifier whose non-inverting input is connected to a resistor to which the respective connection from the control circuit extends so that a voltage is developed across that resistor, in which the output of the operational amplifier is connected to the base of a transistor whose collector-emitter path is in the current feed connection to the appropriate leg of the loop, in which the emitter of said transistor is connected via a resistive impedance to the appropriate power supply terminal and to the inverting input of the operational amplifier, and in which the collector of the transistor is connected via a series diode to its leg of the line.

11. An amplifier as claimed in claim 2, and in which the transistor of the current feed device is a bipolar device.

12. An amplifier as claimed in claim 10, and in which the transistor of the current feed device is a MOSFET.

13. An amplifier as claimed in claim 10, 11 or 12, and in which each said current feed device has a resistive impedance connected in parallel with its emitter-collector path.

14. An amplifier as claimed in any one of claims 1 to 8, in which each said current feed device is a current mirror having its input connected to its respective connection from the control circuit and its output connected to its respective leg of the line.

15. An amplifier as claimed in any one of the preceding claims, and in which for protection purposes two series connected voltage protection clamping devices are connected across the line, the junction of said devices being grounded.

16. An amplifier as claimed in any one of the preceding claims, and which include a voltage sensing device formed by an operational amplifier having its two inputs connected to the two legs of the line, so that its output reflects by the potential thereat the condition of the line.

17. An amplifier as claimed in claim 1, in which the control circuit includes a pseudo long-tailed pair formed by two transistors with their collectors connected together and with the bases forming the inputs to the control circuit from the line and from the reference potential, and output transistors associated with said first-named transistors.

18. A line feed amplifier for feeding the line current to a telephone subscriber's line circuit, substantially as described with reference to Figures 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17 or 18 of the accompanying drawings.

New claims or amendments to claims filed on 25 October 1983

New or amended claims:—

19. A line feed amplifier for feeding the line current to a telephone line circuit, which includes a first current feed device connected between the more positive power supply terminal and a first leg of the line, a second current feed device connected between the more negative power supply terminal and a second leg of the line, a current source which supplies current to a control circuit for the current feed devices, said control circuit including a long-tailed pair whose transistors have their emitters coupled together and to a current source, a first connection from the collector of one of the transistors of the long-tailed pair via which the current supplied by the first current feed device is controlled, a second connection from the collector of the other one of the transistors of the long-tailed pair via which the current supplied by the second current feed device is controlled, a third connection from the base of one of the transistors of the long-tailed pair to a point at a reference potential the value of which depends on the desired operating condition for the line to which the amplifier is connected, and a fourth connection from the line via which a

potential whose value depends on the actual line operating condition is applied to the base of the other transistor of the long-tailed pair, the arrangement being such that variations in line operating conditions cause due, due to comparator action in the control circuit, variations in the currents supplied via said connections to the current feed devices, which variations control the current feed devices to adjust the line currents such that the desired line operating conditions are restored or maintained.

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